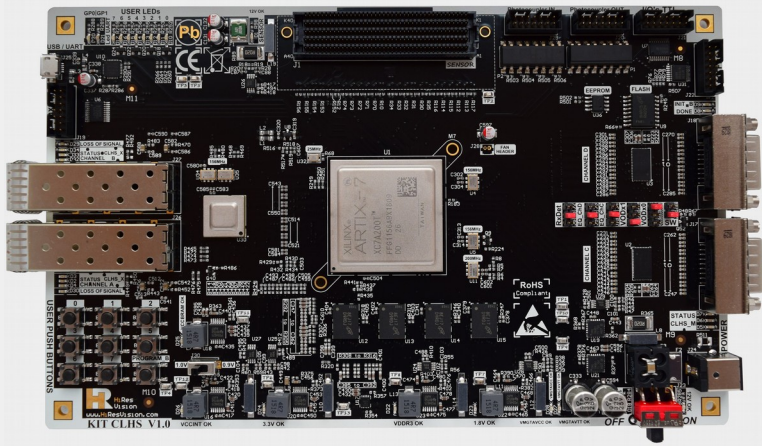




# HIGH RESOLUTION VISION SYSTEMS



## HIRES VISION

INTRODUCES THE FIRST  
CAMERA LINK HS AND  
10 GIGABIT ETHERNET  
DEVELOPMENT KIT

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# DESCRIPTION :

The KIT\_CLHS is a new camera development kit principally oriented to the Camera Link HS 1.0 protocol. Camera Link HS uses copper and fiber optic connectors and cables that were developed for other standards, such as Ethernet.

So the KIT\_CLHS can be easily used for 10 Gigabit Ethernet application and offers an effective solution against CameraLink and GigE Vision protocols limitations.

This kit provides all the necessary components to get the development of embedded vision applications started for both M and X protocols.

The M protocol uses copper cables for applications up to 2.1GB/s and 15 meters long. Active optical cables (AOC) cables are available for systems requiring longer distances of up to 100 meters.

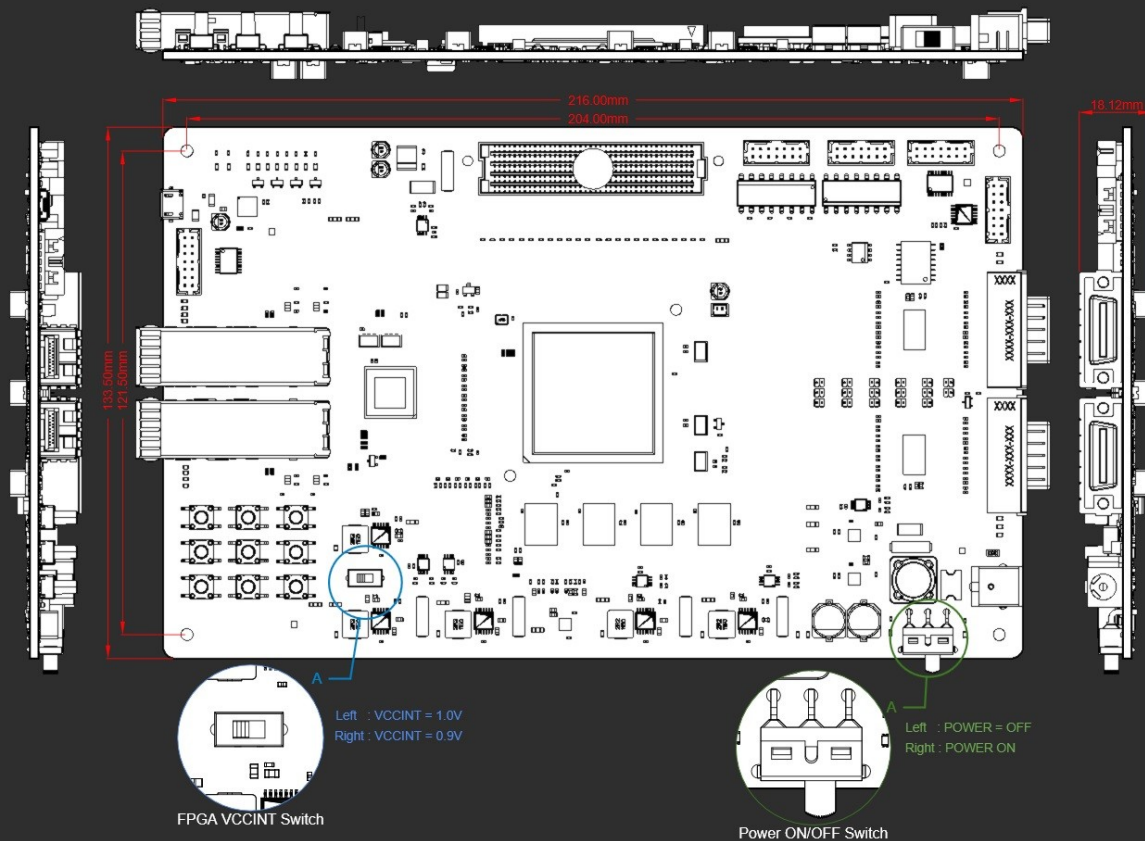
The X protocol (or 10 GigaBit Ethernet) uses fiber optic cables for applications up to 2.4GB/s (2xSFP+ connectors) and 300+ meters long.

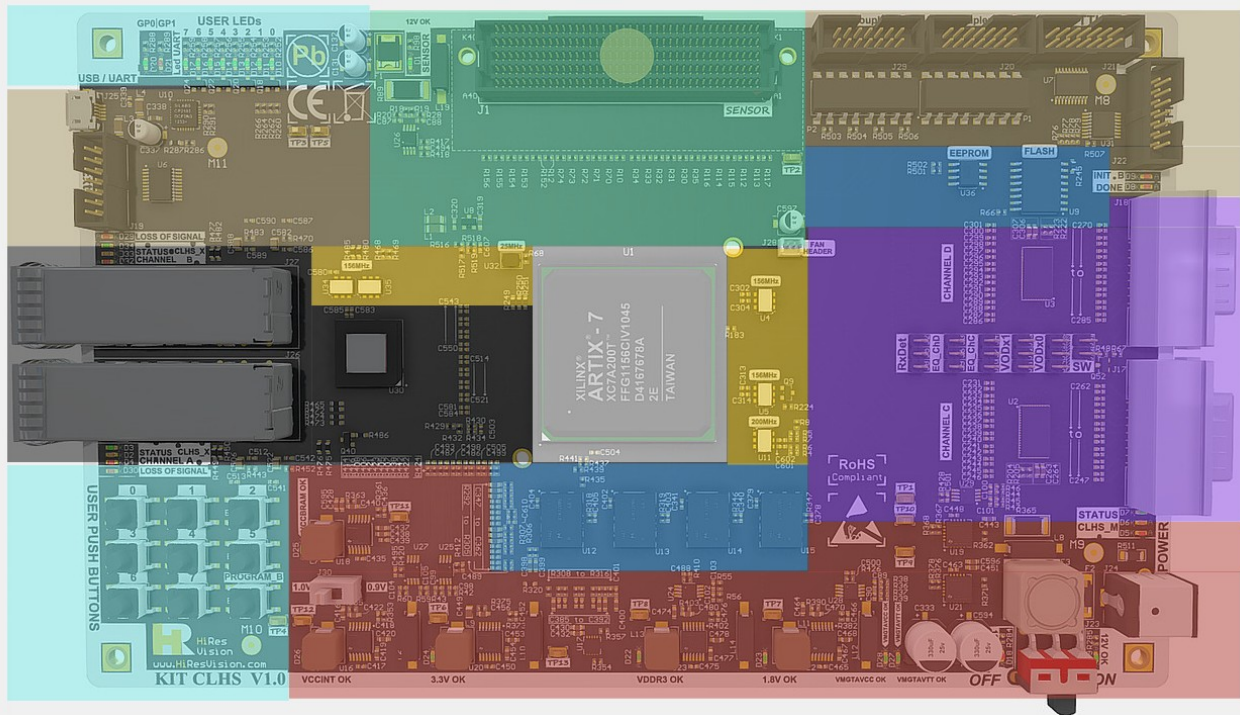
It is a powerful tool focus on camera application ensuring that CMOS sensor technologies can be fully exploited while the provided low-power cameras are low-cost and flexible, and data reliability, as requested by the customers, is guaranteed too.

The main advantage of the KIT\_CLHS is the cost reduction as the time of development of high-performance camera using the protocol CLHS 1.0 and 10 GbE is shortened.

CLHS's IP CORE is available at the AIA and it's evident that IP CORE is enabling the company to save development costs and to shorten development time. Nevertheless, nothing is available as part of the hardware, which is the main advantage of this development kit.

Associated with the CLHS IP CORE provided by the AIA, the development kit offers the perfect solution to greatly simplify development.





## TECHNICAL DATA :

VIDEO OUTPUT	
X – PROTOCOL / 10 GBe	2 x SFP+ connector – 3 led's status for each connector – 1 led "Loss of signal"per connector.
M – PROTOCOL	2 x CX4 connector – 1 for Video transmission with 3 led's status. – 1 for loopback test
MEMORY	
EEPROM	IIC EEPROM 1Mb
FLASH	Quad SPI FLASH 128Mb
DDR3L	4 x DDR3 Low Power 1Gb / 800MHz
CLOCKING	
Fixed oscillator with differential output	1 x 200MHz (DDR3) 4 x 156.25MHz (GTP's)
Fixed Oscillator with CMOS output	1 x 25MHz (GENERAL)
PHYSICAL CHARACTERISTICS	
DIMENSIONS	216 x 133.5 mm
WEIGHT	245 g
CERTIFICATION	ROHS compliant with the European Union Directive 2011/65/EU (ROHS2) CE, UL 94 V-0

INTERFACES	
5 x HEADER	1/ 4 x I2S / SMBUS 2/ 7 x Bidirectional TTL 3/ 4 x Photocoupler Input 4/ 4 x Photocoupler Output 5/ 1 x JTAG Header
USB	UART to USB bridge micro AB Connector
FMC-HPC (Partially Populated)	48 differential pairs up to 1.25Gb/s 20 single-ended signals I2C, 12Volts Power
POWER	12V DC $\pm$ 10 % ON/OFF 2-pos. slide switch
CONTROL / DISPLAY	
PUSH BUTTONS	8 x User Push Buttons (General use) 1x User Push Button (Program_B)
LEDs	8 x User Leds 8 x Leds (Voltage check) 2 x Leds USB/UART GPIO 2 x Leds FPGA configuration (DONE & INIT_B)
FPGA	
XILINX ARTIX-7	Ultra low power FPGA XILINX ARTIX-7 XC7A200T-L2FPG1156E Logic Cell : 215 360 DSP Slices : 740 Memory : 13 140 kb

# 01 FOCUS ON POWER CONSUMPTION

HIRES VISION has chosen the ARTIX-7 Xilinx XC7A200T-L2FGG1156 FPGA for its incomparable low-power consumption capacity. This device provides the highest performance-per-watt fabric.

The FPGA speed grade (-2LE) allows the core tension to be set to two different values:

1.0V (high performance) and 0.9v (ultra-low consumption).

With the latter power reduction of 55% in static and 20% in dynamics are possible compared to a standard C grade.

The system allows measuring all the necessary information for its optimization:

Up to 6 power measurements are possible (FPGA consumption measurement, GTP, DDR3L, FMC connector, 3.3V power rail as well as the total power.)

The measurement of temperature (FPGA) and different voltages are also available.

## *VCCINT = 0.9v* **ULTRA LOW POWER**



**TOTAL BANDWIDTH :**  
**CLHS-X**  
2,4GB/s  
**CLHS-M**  
2,1GB/s - 4,2GB/s

**FMC CONNECTOR**  
**TOTAL BANDWIDTH :**  
5,7GB/s - 7,5GB/s

**DDR3L TOTAL**  
**BANDWIDTH :**  
2,67GB/s - 3,2GB/s

*Compared to C-Grade  
Devices*

## *VCCINT = 1.0v* **HIGH PERFORMANCE**





## 02 FOCUS ON HIGH PERFORMANCE

Full management of the CLHS 1.0 protocol:

\*\* 1 CX4 Connector for the M protocol up to 2.1GB/s bandwidth.

1 Loopback CX4 connector for cable tests.

\*\* 2 SFP+ connectors for X protocol up to 2.4GB/s.

The FPGA reference is the XC7A200T. This reference was chosen because it is the one featuring the most resources. Ideal for heavy applications in image processing.

4 DDR3 low consumption of 1Gb each up to 800MHZ that can provide up to 3.2GB/s total bandwidth.

1 FMC connector for connecting camera interface cards:

\*\* 48 input lvds pair up to 1.2Gb/s for a 57.6Gb/s total bandwidth.

\*\* 20 IO' single-ended useful for the multi-sensor application.

Its FMC connector allows interfacing the card with most of high-resolution or high-speed image sensors. (AMS CMOSIS CMV50000, On Semi VITA 25K, LUXIMA LUX2100....).

## 03 FOCUS ON CAMERA APPLICATION

Most development kits are centered around a particular component and provide the most generic features possible to reach the highest possible market share. It can therefore sometimes be difficult to find the right card with the desired FPGA/SOC with the necessary resources to fulfill its technical specifications. Sometimes pushing some constraints to use cards featuring expensive components, oversized and not suitable for camera applications.

Our development card is perfectly suited for camera applications. Its FMC connector is compatible with a long list of image sensors.

The card has several interfaces :

4 bus I2C, 7 Bidirectional TTL, 4 inputs + 4 optocoupled outputs and 1 USB/UART link.

Thus, it can be interfaced with all types of modules such as lighting system, trigger camera, motor drivers, laser detectors, ....).

The card features also 8 LEDs, 8 push buttons and a 1Kb EEPROM for general applications.

ARTIX-7 family is optimized for lowest cost and power with small form-factor packaging for the highest volume applications. The total bill of materials cost for high-throughput, cost-sensitive applications is the lowest possible one.

While CLHS can run over copper or fiber optic cables, the fiber optics used in telecoms allow a very low-cost application.

## RUGGED SYSTEMS

## 04

The CX4 cable has flex life versions in both copper and fiber and is “industrial” strength. The CX4 is very robust for machine vision, it has thumbscrews and been in use in machine vision for about 8 years.

X protocol uses the 64B/66B coding with Forward Error Correction (FEC) to detect and correct single bit errors and burst errors, which is considerably more secure. As compared to other protocols that don't offer error correction/detection capability, the CLHS protocol corrects errors immediately.

Optical cables are especially attractive since their signal transfer is better. They are not sensitive to electromagnetic interference, they do not produce any interference themselves and they are easy to handle, light and cheap. They feature a very good advantage in an extreme-environment application.

Also, fiber optic cabling is immune to “ground bounce” and so should be chosen for long distances. Ground bounce affects long cable runs and can result in transmission errors.

Additionally, in comparison to copper cables that suffer from induced noise by the flexing/deformation of the cable, fiber has a much higher flex life (over 50 million flex life has been achieved).

All these advantages help ensure reliable image transmission and inspection results.

## FUTURE IMPROVMENTS

## 05

The M protocol is currently limited to transmission speeds of 3.125Gb/s.

This card can allow a fast evolution of the protocol towards frequencies of 5 or even 6.25Gb/s.

This evolution would thus enable to double the bandwidth of the protocol from 2.1 GB/s to 4+ GB/s.

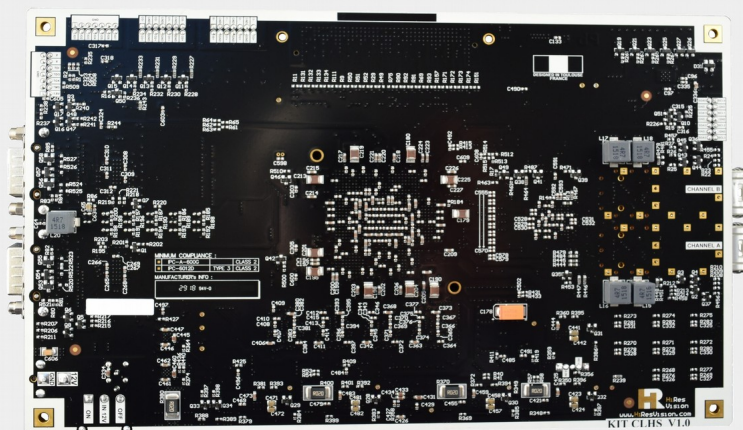
In addition, the card is compatible with some active optical cable just like the ALYSIUM products. This has the advantage of extending the cable distance limit of the current M protocol (15 meters) to higher values in addition to the advantages of the fiber.

The system can retrieve a lot of information about the developed application. It allows to measure the consumption of several parts of the card (such as total power, DDR3, GTP, etc...) and thus provides a good tool for comparing consumption with one of the other protocols.

The set of connectors (M and X PROTOCOL) are doubled, which allows a loopback. This feature makes it possible to fully test the various manufacturer's cables (copper or optical fiber) and to raise their performances (BER, ...). In addition, it provides a tool for measuring the maximum cable distance depending on the transmission frequency.



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